Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**CATHODE**

**CALIFORNIA MFG HAS ANODE ON BACKSIDE**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .004 min**

**Backside Potential: ANODE**

**APPROVED BY: DK DIE SIZE .088” X .088” DATE: 9/1/21**

**MFG: MICROSEMI THICKNESS .009” P/N: 1N5186**

**DG 10.1.2**

#### Rev B, 7/1